Utility Patent Application

Title: **SOLID-STATE HIGH POWER DEVICE**

Inventors:

ZHENQIANG MA
5220 SANDHILL DRIVE
MIDDLETON, WISCONSIN 53562
A CITIZEN OF P.R. CHINA

NINGYUE JIANG
704 EAGLE HEIGHTS, APT. 1
MADISON, WISCONSIN 53705
A CITIZEN OF P.R. CHINA

Assignee:
WISCONSIN ALUMNI RESEARCH FOUNDATION
P.O. BOX 7365
MADISON, WISCONSIN 53707

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Heather S. Sturz

SOLID-STATE HIGH POWER DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The preferred embodiment is directed to solid-state devices, and more particularly, a high power high frequency solid-state device that is heat transfer balanced, and a corresponding method of manufacture.

Description of Related Art

RF power generation has been around for decades. In the early days, such systems employed vacuum tubes as the primary components for providing amplification. However, such systems became impractical for specific applications, e.g., as in mobile phones, and thus an alternative was needed. In this regard, the development of solid-state devices has provided a very capable solution. Today, high power solid-state devices, operational in radio frequency (RF) and specifically the microwave range, are used in a variety of applications, such as in wireless communication systems and radar. Overall, the field of solid-state devices has been critical to the proliferation of products requiring RF power generation, especially those requiring a small package.

In a wireless communication system, the amount of power delivered and the frequency of operation determine the wireless transmission distance and capacity. Moreover, it is desirable, and in fact necessary when designing such a high power device, to not sacrifice the effective operational frequency of the device, especially as the device size is increased to meet the demand for higher power at longer transmission distances. Nevertheless, current solid-state device technology, when scaled for the applications contemplated by the present invention, can only provide either high operation power at the cost of low operational frequency, or high operational frequency but at a substantially reduced power level.

More particularly, with these devices, to improve performance and to make compact circuitry, higher current density and smaller device dimensions have been attempted, however without sufficient care regarding thermal considerations. Such designs usually lead to a higher and localized device temperature rise during operation, which poses a challenge in modeling for circuit design and reliability. To avoid the thermal drawback on the high frequency operating performance, several ideas have been proposed, including using multiple emitter fingers, often with ballasting resistors. Power HBTs (heterojunction bipolar transistors) with multi-emitter fingers with ballasting resistors, can be effective. Usually, emitter ballasting resistors are used for device protection (e.g., minimize thermal run-away effects) and are discussed further below. Notably, their optimal values need to be carefully chosen to insure good thermal instability protection without severe performance degradation. The design of emitter finger spacing is also a tradeoff in view of thermal management, since its reduction can increase thermal coupling between fingers. Overall, in the current state of the art, thermal considerations remain a primary limitation on device performance, and thus a primary concern.

Referring to Figures 1 and 2, solid-state devices for high power applications, such as BJTs (bi-polar junction transistor) and HBTs, typically have three primary components including a base, emitter, and a collector. As noted previously, for high-power devices,

multiple emitter fingers are oftentimes employed to reduce the emitter current crowding effects, etc. In order to increase the power, a bigger device area is required, which is most often accomplished with an array of emitter fingers, which define an emitter area.

Known designs either employ a compact layout (Figure 1), or a distributed layout (Figure 2) in which one or more unit fingers, emitter finger for bipolar junction transistor (BJT or HBT) devices and gate finger for field effect transistor (FET) type devices, are grouped in a single cell. In both layout structures, the unit fingers or unit cells are arranged in a uniform spatial distribution. In the compact layout of Figure 1, for example, device 10 includes a base 12, an emitter 14 and a collector 16. Emitter 14 includes ten emitter fingers 18 (e.g., for an HBT) as shown, with each adjacent finger 18 along the line or row of emitter fingers 18 being separated by an equal perpendicular distance "X". In the distributed layout of Figure 2, device 20 includes a base 22, an emitter 24 and a collector 26. Emitter 24 includes three sub-cells 28 where adjacent ones of sub-cells 28 include two emitter fingers 29 each and are separated by an equal distance "Y" (defined between two edges of adjacent sub-cells), i.e., they are uniformly spaced along the row in which they lie. Within each sub-cell, the emitter fingers are separated by a distance "X", as in the compact layout (Figure 1).

During operation of the high power devices, each unit finger or cell is a power source with corresponding heat generation. Because the paths of heat dissipation and transfer for all the unit power sources are different in each large device layout, this uniform distribution of the unit fingers or cells yields a non-uniform distribution of junction temperatures across the device.

An example of this result is illustrated in Figures 3A and 3B. In Figure 3A, a thermal image of a device 30 having five sub-cells 32 of emitter fingers is shown. Notably, upon running a simulation program the thermal profile can be imaged as shown in Figure 3A. The dark regions near the center indicate hot spots in the device. The temperatures associated with this image are graphed in Figure 3B, where it is clear that

the temperature distribution across the device varies in a non-uniform fashion. Most notably, emitter finger sub-cell 34 shows the hottest region of the device with the flanking cells near the edges of the device exhibiting a junction temperature significantly lower.

This non-uniformity of junction temperature distribution across large-sized devices causes problems such as thermal instability, and reduced current gain of heterojunction bi-polar transistors and the transconductance gain of field effect transistors, thus limiting the large signal swing amplitudes and the power handling capability of these devices. See, for instance, Figure 4 corresponding generally to the device shown in Figure 1. In this case, power handling capability is particularly limited at the center "C" of the device where heat dissipation is the lowest.

The hot spots of the junction temperature also degrade the mobility and drift velocity of carriers and thus decreases the frequency response of these large sized power devices. And, with more unit fingers or cells incorporated in the power device, the higher the non-uniformity of the junction temperature distribution across the device, and thus the slower the frequency response. Overall, the operational frequencies of any large sized power device using these conventional layout structures, such as those shown in Figures 1 and 2, are always significantly lower than their unit finger/cell low-power counterparts of the same device structure.

Notably, the type of substrate employed also affects frequency response, where a design using a pure silicon substrate can achieve a frequency response of 1 to 10 Gigahertz, for example. More particularly, "high frequency" for high power in the present preferred embodiments typically refers to a higher frequency range in which a particular type of solid-state device can operate. For different devices made of different materials, such higher frequency ranges for power amplification can be quite different. For example, with pure Si, from DC up to 1.5 GHz, "high frequency" may represent 100 MHz-1.5 GHz. Note that by comparison a Pentium® microprocessor already operates at

3.5 GHz using pure Si, but the devices in this microprocessor are not power devices. Next, with a SiGe substrate, from DC up to 12-20 GHz, "high frequency" may represent 1.5-20 GHz. For GaAs from DC up to 30 GHz, "high frequency" may represent 1.8-30GHz. Finally, with an InP substrate from DC up to 100 GHz, "high frequency" may represent 5-30 GHz.

To try to overcome the operational frequency problem, as noted earlier, unequally valued ballasting resistors (see, for instance, resistors 19 in Figure 1, and resistors 27 in Figure 2) are connected to the emitter fingers to limit the current level by providing a negative feedback mechanism and to achieve uniform distribution of junction temperature. When considering multi-emitter finger BJTs and HBTs, at low collector current, the device has a typical I-V thermal drop and breakdown. However, at higher levels of current, a sharp drop in current typically occurs with increasing voltage. Considering multi-finger BJTs and HBTs that are built on substrates having poor thermal conductivity, such as GaAs or InP devices, the reason typically is current "hogging" by a localized hot spot region at one or more of the emitter fingers, with the turn-on voltage being controlled by the energy gap rather than the emitter resistance. As a result, there is an overall current reduction in the other emitter fingers. Emitter ballast resistors (19, 27) are therefore used in HBTs to also maintain more uniform emitter-base turn-on voltages for devices with multi-emitters, and to increase the threshold for thermal runaway. Typically, for reasons discussed above, higher valued resistors are added in the center of the device, while the emitters at the edge of the device are provided with resistors having lower values. Thermal stability and uniformity of the junction temperature can be achieved in this way; however, both the frequency response, due to the added extra resistance and the power handling capability (due to reduced biasing) are sacrificed, as is appreciated by those skilled in the art.

In sum, thermal effects of the device are the dominant factors that limit the high frequency response and power handling capability of large- sized power devices. A design that minimizes or completely eliminates these adverse effects was therefore

desired. More particularly, the art of solid-state devices was in need of a design and/or fabrication technique that maximizes the power handling and frequency range of solid-state power devices to fully exploit the potential of such devices for particular applications, such as wireless communication and radar.

SUMMARY OF THE INVENTION

The preferred embodiment overcomes the drawbacks of known systems by heat transfer balancing the device. More particularly, for these high-powered devices, the sub-cells of the corresponding device are spaced in a non-uniform fashion to provide a more uniform junction temperature across the device. The number and spacing of the sub-cells containing emitter fingers (e.g., for BJTs) are determined by running a simulation program, with the maximum number of fingers per sub-cell depending on the finger width and the power density of the fingers. The spacing between the sub-cells and whether more than a single row of sub-cells should be used in the design may also be determined by running the simulation program. If more than one row of sub-cells is used in the design, the spacing between the sub-cells in two dimensions must also be determined for optimum performance. Overall, the total number of fingers determines the total power output of the device. Again, the longer the wireless transmission distance must be, the higher power required, and thus the more fingers required. The ultimate design will depend on the particular application characteristics with, in each case, the sub-cells being spaced so that consecutive adjacent pairs of sub-cells are spaced a different distance. By doing so, no ballasting resistors are required.

According to one aspect of the preferred embodiment, a solid-state device includes a terminal having a plurality of fingers. In this device, the fingers are arranged so that the device is heat transfer balanced. In another aspect of this embodiment, the fingers are arranged in a row and are spaced non-uniformly in the row.

According to another aspect of this preferred embodiment, each of the fingers is associated with a corresponding one of a plurality of sub-cells. In addition, the sub-cells are arranged in a row and spaced non-uniformly. Also, each sub-cell may include one finger.

In a further aspect of this preferred embodiment, the device has a terminal area defining opposed edges. In this case, adjacent ones of the sub-cells are spaced a greater distance at or near the center of the device than at or near the opposed edges.

In another aspect of this preferred embodiment, each of the fingers is associated with a corresponding one of a plurality of sub-cells, wherein the sub-cells are spaced so that at least one of consecutive adjacent pairs of the sub-cells are spaced differently. Moreover, the sub-cells may be placed in two or more rows depending upon the application parameters.

Moreover, multiple sub-cells may be used in a power device. In this case, fewer fingers are typically placed in the sub-cell(s) that lie at or near the center of the device. And, more fingers are placed in the sub-cells that lie near the edge of the device. Again, the sub-cells are arranged in a way such that a general uniform junction temperature is obtained across the device.

According to yet another aspect of the preferred embodiment, a solid-state device includes a terminal having a plurality of fingers. In this case, the fingers are arranged so that a peak oscillation frequency, f_{max}, associated with the device is much less dependent on the number of fingers. In the end, higher operation frequencies can be achieved without sacrificing the power level. In another aspect of this embodiment, the device is an HBT, and the fingers are emitter fingers.

According to a further aspect of the preferred embodiment, a method of producing a high power solid-state device includes providing a substrate for supporting a terminal having a plurality of fingers. In addition, the method includes arranging the fingers in a plurality of sub-cells defining at least one row so that the device is heat transfer balanced, i.e., a generally uniform junction temperature across the device.

In another aspect of this embodiment, the sub-cells are arranged so that consecutive adjacent pairs of the sub-cells in the at least one row are spaced differently.

According to another aspect of this embodiment, the at least one row includes a plurality of rows. In addition, the sub-cells between the plurality of rows are spaced non-uniformly. Moreover, the method includes the step of determining a number of sub-cells and spacing between the sub-cells using a thermal simulation program. Preferably, the thermal simulation program uses finite element analysis.

According to another aspect of this embodiment, the device is a multi-emitter finger BJT or HBT, and the device defines a layout that is ballasting resistors-free.

According to yet another aspect of the preferred embodiment, a method of heat transfer balancing a solid-state device includes arranging a plurality of fingers of a terminal of the device so that a junction temperature across the device is generally uniform without using ballasting resistors.

In another aspect of this embodiment, each finger is biased for its maximum current density during operation. If the device is an BJT or HBT, the terminal is an emitter terminal. Notably, the preferred embodiments using heat transfer balancing work equally as well in the design of FET devices, such as power MESFET or power HEMT and others.

These and other objects, features, and advantages of the invention will become apparent to those skilled in the art from the following detailed description and the accompanying drawings. It should be understood, however, that the detailed description and specific examples, while indicating preferred embodiments of the present invention, are given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred exemplary embodiment of the invention is illustrated in the accompanying drawings in which like reference numerals represent like parts throughout, and in which:

Figure 1 is a top plan view of a prior art solid-state device layout for a device having a plurality of emitter fingers, in a compact layout;

Figure 2 is a top plan view of a prior art device layout having emitter fingers arranged in cells, in a distributed layout;

Figure 3A is an image of a device similar to the distributed layout shown in Figure 2, illustrating junction temperature associated with five sub-cells disposed in a single row;

Figure 3B is a graph depicting the temperature distribution for the device corresponding to the image shown in Figure 3A;

Figure 4 is a graph depicting the low power handling capabilities of the devices shown in Figures 1 and 2;

Figure 5 is a top plan view of a solid-state device layout according to a preferred embodiment, wherein the emitter fingers are arranged in cells that are separated in a non-uniform fashion;

Figure 6A is a thermal image of a device of an alternate device layout according to the preferred embodiment;

Figure 6B is a graph depicting the junction temperature distribution for the device corresponding to the image of Figure 6A;

Figure 7A is a thermal image of a device of another alternate device layout according to the preferred embodiment;

Figure 7B is a graph depicting the junction temperature distribution for the device corresponding to the image of Figure 7A;

Figure 8A is a thermal image of a device of yet another alternate device layout according to the preferred embodiment;

Figure 8B is a graph depicting the junction temperature distribution for the device corresponding to the image of Figure 8A; and

Figure 9 is a graph showing the frequency response of a solid-state device according to the preferred embodiment, in comparison to that of prior art designs.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Turning initially to Figure 5, a top plan view of a device layout 50 which is heat transfer balanced according to a preferred embodiment including sub-cells 52 each having a pair of emitter fingers 54 is shown. Notably, in this example, the sub-cells 52 lie in a single row across and are non-uniformly spaced or distributed, and define a terminal region, h x w, for example. More particularly, for HBT and BJT devices, the terminal region is defined by the emitter area, which depends on the number of fingers, the width of the fingers, and their length. When building FET-type devices, the terminal region is defined by gate width, where length is a speed parameter and width is a power parameter.

As an example, a total emitter area of 100 μm^2 may generate about 100mW RF power for SiGE HBTs, and about 150-200mW for III-V HBTs. Of course, power handling capabilities also depend on device vertical structure (e.g., collector doping).

With further reference to Figures 1 and 2, adjacent sub-cells of two emitter fingers 54 each are non-uniformly spaced, and are separated by distances corresponding to X_1, X_2, and X_3. Notably, in this case, X_1 is greater than X_2, which is greater than X_3. The center sub-cells 52 are preferably spaced the greatest distance due to the fact that the adverse heating effects caused by a multi-emitter layout are the greatest in the center of the

device. Not only does this design overcome the detrimental thermal effects, the parasitic collector resistance associated with the compact layout in large-area power devices is also substantially reduced. Notably, this heat transfer balanced layout provides a uniform distribution of the junction temperature with each emitter finger biased for its maximum current density, without the need for ballasting resistors, thus providing optimum performance in terms of both power level and frequency response.

More particularly, the maximum power handling capability of the device (for example, an HBT) is realized, contrary to known devices that perform typically as shown in Figure 4. Moreover, the scalability of the frequency response for large-area solid-state devices, such as a SiGe HBT, is achieved by realizing lower junction temperature across the device. As a result, such devices can be readily implemented for high-frequency (e.g., microwave) power amplification.

The way in which the variables (e.g., spacing and cells) are determined is application specific and is accomplished by executing simulation software (for example, software using finite element analysis) to determine the distribution of junction temperature across the device, and thus insure that the layout is heat transfer balanced. In this way, the user empirically selects a number of cells, a number of emitter fingers per cell, and a spacing between the cells ($X_1, X_2 \ldots, X_n$) given the application parameters, such as power handling capability, so that optimum performance may be achieved. Overall, in the preferred embodiment, for a single row of emitter fingers, the heat transfer balanced layout provides a quantitative solution based on an empirical determination of the above parameters (e.g., number of fingers in a sub-cell, the space in between every two adjacent cells and the total number of sub-cells). Alternatively, the selection may be automated with the user selecting parameters associated with their application which are processed to identify a number of sub-cells, spacing, etc. which is then tested via the simulation program. In either case, a heat transfer balanced design for optimum performance is achieved. Example designs are illustrated in the following figures 6A, 6B, 7A, 7B, 8A and 8B, and described below.

With reference to Figure 6A, a device 60 (in this case, an HBT) is heat transfer balanced using a simulation program to empirically determine the emitter variables set forth above (e.g., cells, fingers, spacing, etc.). As shown in the top plan view of Figures 6A and 6B, junction temperature is clearly more uniformly distributed than that shown in Figure 3B, corresponding to the known non-heat transfer balanced design, including uniform spacing of the emitter sub-cells. More particularly, the temperature image of Figure 6A illustrates ten sub-cells 62 having, for example, one emitter finger each, with each sub-cell 62 spaced from an adjacent sub-cell unequally, where X_2 is less than X_1, and so forth. Notably, although the row of sub-cells is shown generally symmetrical about a mid-point 64 of the row, this is not necessary. The key is that consecutive adjacent pairs of sub-cells in a row are spaced differently, in a non-uniform fashion. Also, although Figures 6A and 6B have been described in terms of using sub-cells, the sub-cells may include any number of emitter fingers, including one.

With this design, it is clear that with more sub-cells of emitter fingers spaced in a non-uniform fashion, the thermal distribution is much greater than the design depicted in Figures 3A and 3B. Superior performance in terms of power and frequency response is thus achieved.

Next, with reference to Figures 7A and 7B, the heat distribution is improved even further with the alternate design illustrated. In this case, device 70 includes two rows 72, 74 of ten sub-cells 76 having one emitter finger each (best shown in Figure 7A). The sub-cells 76 are disposed adjacent to each other, with the sub-cells 76 of each row being non-uniformly spaced, i.e., consecutive adjacent pairs of sub-cells 76 are spaced differently. In this case, a second dimension, Y, corresponding to the spacing between sub-cells 76 of each row must be determined, again preferably empirically using simulation software yielding thermal distribution across the device. Therefore, spacing in two-dimensions (X and Y, as illustrated in Figure 7A), corresponding to spacing both within their respective rows and between rows must be considered in this application. Again, the variables (e.g., the number of sub-cells, emitter fingers and spacing) are determined based on the parameters of the particular application being implemented, with

the user selecting different combinations of the variables and running the simulation software to yield a thermal image distribution. In this case, as shown in Figure 7B, the junction temperature varies no more than about 2° K. With such a design, the power handling capability is optimized with no compromise of frequency response. Note that the term "row" is used herein for convenience purposes, and that rows of emitters may exist along non-linear lines, as shown in Figure 7A. The connections between emitters, bases and collectors in sub-cells can be achieved using minimal conventional multi-level interconnects, as appreciated by those skilled in this art.

In Figures 8A and 8B, an alternate design 80 is shown employing thirty sub-cells 82 with one finger of each that are placed in three rows 84, 86, 88 and are non-uniformly spaced, both in "X" and in "Y." Because the thermal profile of the device at its center is the most difficult to control, the center row 86 includes eight sub-cells 82 while the flanking rows 84, 88 adjacent thereto each include eleven sub-cells 82. By executing the thermal simulation program, the variables, including the number of emitter sub-cells 82, the number of rows in which they are placed, and the spacing both between the sub-cells 82 within the rows and between the rows, are determined and the heat distribution shown in Figure 8B is achieved. Note that the graph of Figure 8B corresponds to junction temperature along the center row 86. Of course, any number of device layouts may be employed to meet the user's design characteristics by running the design through the simulator to provide a thermal profile. In this way, the number of sub-cells, the number of emitter fingers per sub-cell, the rows in which they are placed, and the spacing between the fingers in two dimensions (X_1, X_2,...and Y_1, Y_2, ...) can be determined for optimized performance based on the design parameters of the application. In each case, however, non-uniform spacing of the sub-cells in one or two dimensions is critical, and allows for a layout that is ballasting resistors-free, thus significantly improving the frequency response of the device.

By adding the "Y" variable in the design, some (really not much) chip area can be saved. In general, the case utilizing the "Y" variable shows that an "absolute" uniform

junction temperature across the entire device area can be achieved using the present design method.

In sum, the design variables of design may include: 1) number of fingers per sub-cell (if one finger per sub-cell is used in particular, then the number of fingers will be the same as the number of sub-cells, with the maximum number of fingers per sub-cell depending on the finger width) 2) number of sub-cells; and 3) spacing between the sub-cells. If many fingers are needed for high power operation and a single row layout does not yield heat transfer balancing as described herein, then more variables may be included: 4) the number of rows; 5) the number of sub-cells associated with each row (can choose equal number, but equal sub-cells is not necessary); and 6) the spacing between rows.

In the end, the total number of fingers generally determines the total power output. Higher power will allow longer wireless transmission distance, which depends on the application. Of course, some applications only need low output power, and even for these cases, heat transfer balancing according to the present preferred embodiment provides improved performance in terms of frequency response.

Turning to Figure 9, a profile of the peak frequency in gigahertz versus the number of emitter fingers is shown for devices designed according to the preferred embodiment (Figure 6A, 6B, 7A, 7B, 8A and 8B), as well as prior art devices. As shown, for the conventional compact layout (see Figure 1), the more emitter fingers employed in the design, which is application specific, the lower the frequency response, thus limiting its range of applications. In the distributed layout (see Figure 2), including sub-cells of two emitter fingers, the number of emitter fingers again compromises the frequency response. Nevertheless, even with the distributed layout, the frequency response deteriorates with the greater number of emitter fingers. To the contrary, with the preferred embodiment, the layout demonstrates negligible f_{max} degradation with an increase of device power level, i.e., with an increased number of emitter fingers. This is in direct contrast to both the conventional compact layout and the distributed layout, and

provides optimum frequency response as the device area becomes larger (i.e., as power requirements increase).

Although the best mode contemplated by the inventors of carrying out the present invention is disclosed above, practice of the present invention is not limited thereto. For example, although the preferred embodiments have been mostly described in conjunction with the fabrication of HBTs, the preferred embodiments are applicable to fabricating multi gate finger FETs. It will be manifest that various additions, modifications and rearrangements of the features of the present invention may be made without deviating from the spirit and scope of the underlying inventive concept.